Exploring Low Loss Suspension Interconnects for High Data Rates in Hard Disk Drives

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Question #1
Can current interconnect technology support the push towards 3Gb/s internal data rates?

Answer #1
YES . . . Today’s interconnect technology can support the push towards 3Gb/s internal data rates.
Question #2

Future interconnects – What are their features and benefits?

Answer #2

Future low impedance, high bandwidth interconnects can enable lower power and lower voltage writer front ends.
Outline

• Writer Interconnect Functions
• Today's Suspension Interconnects and Corresponding Design Space
• Writer Front End System Model:
  • Experiment #1 - Current Interconnect Technology Supports 3 Gb/s Data Rates
  • Experiment #2 - Benefits of Low Impedance/High Bandwidth Interconnects
• Low Impedance and High Bandwidth Interconnect Structures and Design Space
Interconnect Functions

Lower Power:
- Lower total system power use during write

Signal Integrity:
- Need high signal integrity for write current waveform (low loss and constant impedance)
  - Need to preserve low mechanical stiffness without introducing impedance discontinuities

Manufacturability:
- Interconnect must be easy to make in high volume!
Today’s Interconnect – Differential Microstrip

- Typically a designer will change trace width, spacing or the stainless steel backing percentage to adjust for impedance.

\[
Z = \frac{Voltage}{Current} \approx \sqrt{\frac{L}{C}}
\]

- SST losses limit bandwidth by \(~ 1 \text{ to } 2 \text{ GHz}\) in fully backed structures.
- Windowing allows for increased interconnect bandwidth, but increases \(Z_{\text{diff}}\).

**Differential Microstrip Cross Section**

- SST losses limit bandwidth by \(~ 1 \text{ to } 2 \text{ GHz}\) in fully backed structures.
- Windowing allows for increased interconnect bandwidth, but increases \(Z_{\text{diff}}\).

**INSERTION LOSS** (signal loss vs. frequency)

**Coupons produce design space shown on next page (current microstrip interconnect)**
Current Microstrip Interconnect – Design Space

Remove stainless steel to increase bandwidth
Writer Front End System Model

Experimental Model…

• Write Driver: Experimental Preamp (~100 ps rise time, target 3Gb/s internal data rate)
• Write Interconnect: Measured Interconnect Coupon
• Write Head: Generic PMR Head Model Based On Measurement
Experiment #1:
Today’s Interconnect Structure Capability

Experiment #2:
Future Interconnect Structure Capabilities
Experiment #1
66 Ohm Interconnects With Variable Bandwidths

More stainless steel windowing and wider traces gives same impedance but higher bandwidths.
Experiment #1
66 Ohm Interconnects With Variable Bandwidths

- Recent write source $Z_{\text{diff}}$ is between 55 Ohm and 70 Ohm for high data rate preamps

- 30 mA increase in peak current overshoot going from 1.5 GHz to 8.5 GHz

- One aspect of high bandwidth interconnects is that secondary reflected pulses occur at head 2 time delays after initial pulse
Experiment #1

_Rise Time, Launch Voltage, Power Dissipation vs. BW at 66 Ohm Interconnect_

**DR = 3 Gbps, I_w-pk = 100 mA**

**Z_o = 66 ohms; BW = 1.5, 2, 3.25, 6.0, and 8.5 GHz**

![Graph showing the relationship between bandwidth, rise time, power dissipated, and launch voltage.](image-url)
Experiment #1: Today’s Interconnect Structure Capability

Experiment #2: Future Interconnect Structure Capabilities
Experiment #2
Variable Impedance, Constant BW Coupons

Achievable through alternate interconnect structures
Experiment #2
Variable Impedance, Constant BW Coupons

- 70 mA increase in peak overshoot current going from 90 Ohm to 25 Ohm interconnect impedances
- 62 Ohm and 71 Ohm shows best convergence to steady state, which is an effect of preamp/interconnect matching
Experiment #2

Launch Voltage & Pd vs. Zdiff at 8 GHz BW

DR = 3 Gbps, Iw-pk = 100 mA

BW = 8 GHz; Interconnect Zdiff = 25, 40, 62, 71, 90, and 101 Ohm
Alternate Interconnect Structures

**Copper Ground Plane**
- Thin copper layer reduces stainless steel losses
- Suffers from same impedance/bandwidth tradeoff as today’s interconnects

**Stacked Traces**
- Trace width and separation determine impedance
- Separation determines interconnect bandwidth almost exclusively

**Interleaved Traces**
- Increases the number of differential coupling traces
- Produces half the impedance of a standard Cu-Poly-SST windowed structure, but same bandwidth
Question #1
Can current interconnect technology support the push towards 3Gb/s internal data rates?

Answer #1
66 Ohm impedance/variable bandwidth experiment shows that today’s interconnects can support the push towards 3Gb/s internal data rates.

Question #2
Future interconnects – What are their features and benefits?

Answer #2
Future interconnects will be low impedance, high bandwidth interconnects that enable lower power and lower voltage (i.e. more efficient) writer front ends.
HTI looks forward to working with the entire HDD supply chain to meet future high data rate requirements. Thank you for attending today’s presentation.