Phase Change Memory:
From Concept to Product

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History of Phase Change Memory
The Concept

- Stan Ovshinsky first filed a patent on June 21, 1961 on the switching between high and low resistance states for electrical circuits.
- In the first granted patents 3271591, he demonstrated the many different ways the circuits could be fabricated.
- Reversible electrically induced changes in the resistance of thin films of chalcogenide alloy amorphous semiconductors were first reported in the technical literature in 1968.
One of the First Attempt

1970

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die</td>
<td>122 mil X 131 mil</td>
</tr>
<tr>
<td>Capacity</td>
<td>256 bits</td>
</tr>
<tr>
<td>Reset</td>
<td>( \sim 200 \text{ mA} ), &lt; 25V, ( 5 \mu\text{s} )</td>
</tr>
<tr>
<td>Set</td>
<td>5 mA, ( \sim 25V ), 10 ms</td>
</tr>
<tr>
<td>Read</td>
<td>2.5 mA, &lt; 5V</td>
</tr>
</tbody>
</table>

Detour in Phase Change Memory

- With the large current and slow switching, phase change memory was not competitive with EPROM, and the semiconductor memory industry lost interest.
- Optical memory application of laser-initiated reversible phase-change in chalcogenide alloy films was reported in 1971.
  
- In the 80’s and 90’s, there was intense effort in Japan for development of RW CD/DVD which perfected the GST material.
- In 1999, Ovonyx was founded to take a fresh look at the new material in electrical memories.
Progress in Phase Change Memory

1. Use of fast-crystallizing alloys (mS -> nS)
2. Electrode/chalcogenide size reduction and cell thermal optimization
Phase Change Memory Capability
Basic Memory Concept

- **Amorphous Phase**
  - TEM Images
  - Short-range atomic order
  - Low free electron density
  - High activation energy
  - High resistivity

- **Crystalline Phase**
  - Electron Diffraction Patterns
  - Long-range atomic order
  - High free electron density
  - Low activation energy
  - Low resistivity

- **Operation**
  - Chalcogenide material alloys used in re-writable CDs and DVDs
  - Current provides heat that converts the material between crystalline (conductive) and amorphous (resistive) phases

- **Attributes**
  - Non-volatile & high density
  - Direct fast write & bit alterable
  - ~10^{12} write/erase cycles
  - Non-destructive fast read
  - Low voltage operation
  - Integrate-able w/ CMOS logic
Basic Memory Element

- Memory cell = memory element (variable resistor) + selector
- Selector can be MOSFET, BJT, Diode or other switches
A Memory For Everybody

- Even though Phase Change Memory is not an universal memory in all respects, it comes close to an universal memory on how it can be used.
- For embedded with the smallest amount of process change, one can get a high cycle EEPROM equivalent at lower cost.
- By using the same process but changing the alloy, one can get a high temperature memory suitable for the most demanding automotive application.
- For dedicated high density memory, one can get a memory cell that is smaller than DRAM and has multi-level cell capability. Using high performance alloys, programming speed similar to DRAM are available.
- Using special switched selectors, one can get multi-layer memory than can rival NAND memory in cost.
Technology Capability

- Direct write capability (no erase before write) as well as byte function (no block flash erase) makes it RAM like, easing significantly system implementation
  - For flash, changing a byte involves saving the current data, erasing a whole block (>100 mSec) and writing back old data + new byte (total ~1 sec)
  - For PCM, changing a byte involves writing the new data: (total < 100 nSec, can be less than 50 nSec with new alloy)
  - Endurance >> $10^8$ cycles

- With read current > 10 $\mu$A, read speed is expected to be comparable to NOR and DRAM
Potential: DRAM Cost

- Samsung has demonstrated a 5.8 l2 memory cell using selective epi diode as selector.
- The simple memory cell structure scales directly with lithography
- Multi Resistance levels are possible

- We believe this cell structure can achieve competitive cost with DRAM.
- Read performance can be improved through array architecture. Key challenge is write performance and is addressed with newer high performance alloys.
Samsung 512 Mb

Figure 2. A photograph of 512Mb PRAM chip.
Material Scaling Limit

Phase Change Mechanism Appears Scalable to at Least ~5nm

Can We Reach Tbit/sq.in. Storage Densities With Phase-Change Media?
C.D. Wright, M. M. Ariz, M. Armand, S. Sonkader and W. Yu
Department of Engineering, University of Exeter, UK

![Graph showing minimum stable size vs. temperature]

- 14nm pitch 3.3Tb/in²
- 20nm pitch 1.6Tb/in²
- 40nm pitch 0.4Tb/in²

Crystalline Bits in Amorphous Matrix.

Source: C.D. Wright et al., EPCOS 2004
Source: C. Lam, SRC NVM Forum 2004
Market Opportunity

- Market growth is expected to be over different phases driven by cost
- First adopters to value performance (direct write, byte function, cycles)
- As cost comes down, it will penetrate NOR, then DRAM and eventually NAND markets over probably 5+ years
- More than just replacement of current NV memories, the new capability, both in terms of performance and cost, will create new market and new growth opportunities
- Most interesting new market is PCM in PC
Summary

- Phase change memories based on Chalcogenide accepted by industry as leading candidate for new NV memories
  - Ovonyx licensees: Intel, STM, Elpida, Samsung, Qimonda + others not disclosed or in discussion
- Near term: higher functionality (easy CMOS add on, direct byte write instead of block, > $10^6$ Cycles) makes a better flash
- Longer term: more scalable, cost cross over NOR, then DRAM, then NAND as NOR/DRAM/NAND slow down in scaling