On the Design of Iterative Codes for Magnetic Recording Channel

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Outline

• Two classes of Iterative architectures
• RS-plus Iterative architecture
  – Code design methodology
  – Examples
  – Simulations results
• RS-less Iterative architecture
  – Code parameters
  – Simulations results
• Concluding remarks
Iterative Architecture Classes

- There are two types of Iterative architectures suitable for application in magnetic recording channel:
  - *RS-plus iterative architecture*. Concatenation of outer RS ECC code with inner iterative code.
  - *RS-less iterative architecture*. A strong Iterative code is the only ECC that provides data reliability.
RS-plus Iterative Architecture Class

512 bytes → 10-bit RS ECC encoder → Iterative Code encoder → Channel

10-bit RS ECC decoder → Iterative Code decoder → SOVA

RS ECC SER is the ultimate measure of performance

Inner iteration → Outer iteration
RS-less Iterative Architecture Class

Iterative Code encoder → Channel

Iterative Code decoder

Inner iteration

SOVA

Outer iteration

Iterative Word ER is the ultimate measure of performance
RS-plus Iterative Architecture

• Desirable Inner Iterative Code Characteristics
  – Iterative code has to have symbiotic relationship with outer RS ECC decoder. Error signature at the output of iterative decoder is very important: must not have any long error bursts (here burst length is measured in RS ECC symbols) at the output of iterative code.
  – This favors use of “weaker” iterative codes as components of RS-plus iterative architecture.

• In this presentation we consider two RS-plus Iterative architectures based on
  – Interleaved Single-Bit Parity Code (ISPC)
  – Turbo Product Code (TPC-SPC)
TPC-SPC

RS ECC encoder

n

interleaver

Parity bits

Parity bits

MUX

d_{min}=4

Parity bits

Channel

RS ECC decoder

Min-Sum Iterative Code decoder

3x per outer iteration

SOVA

5 outer iterations

8
• For RS-plus iterative architecture, it is important to achieve good redundancy allocation between outer RS ECC decoder and inner Iterative decoder.
  – In practice, the choice of RS ECC correction power is primarily driven by necessity to handle long TA’s and media defects.
  – For RS Iterative architecture, iterative code is not strong enough to handle TA’s and media defects, therefore this task falls onto outer RS ECC code.

• The following two slides shows the performance of RS-plus iterative code with RS ECC optimized for defect handling, t=24 symbols.
Performance of RS-plus Iterative Architecture With Random Noise

Perp. channel, NPV=[4,7,1], UBD=1.1, jitter=90%, RS-plus Iterative Architecture

- TPC-SPC gains ~3.0 dB over 60/61 SPC @ SyER=3e-4
- ISPC gains 1.0 dB over 60/61 SPC @ SyER=3e-4
Performance of RS-plus Iterative Architecture With Random Noise

Perp. channel, NPV=[4,7,1], UBD=1.1, jitter=90%, RS-plus Iterative Architecture

• TPC-SPC gains 0.2dB over 60/61 SPC @ SER=1e-5

• ISPC gains 0.1 dB over 60/61 SPC @ SER=1e-5
Performance of RS-plus Iterative Architecture With Random Noise

• RS-plus Iterative architecture often performs better with weaker outer RS ECC code (correction power in low teens) in random noise environment.

• The following two slides shows the performance of RS-plus iterative code with RS ECC optimized for random errors, t=12 symbols.

• In practice, reducing RS ECC correction power is not a viable option since defects are relatively frequent in the existing drives.
Performance of RS-plus Iterative Architecture With Random Noise

- **TPC-SPC + RS(t=12) gains**
  ~3.5dB over 60/61 SPC @ SyER=1-e4

- **TPC-SPC + RS(t=12) is 0.5dB better than TPC-SPC + RS(t=24) @ SyER=1-e4**
Performance of RS-plus Iterative Architecture With Random Noise

- TPC-SPC +RS(t=12) gains ~0.7dB over 60/61 SPC+RS(t=24) @ SER=1*e4.

- TPC-SPC code SER curve does not drop as fast as other codes.
Performance of RS-plus Iterative Architecture With Media Defects

- Media defect model

![Diagram]

0 \leq \alpha \leq 1

AWGN noise
Performance of RS-plus Iterative Architecture With Media Defects

defect length 50 bits, attenuation alpha=0.5
Perp. channel, NPV=[4,7,1], UBD=1.1, jitter=90%, RS-plus Iterative Architecture

- All RS-plus iterative codes perform poorly with media defects
- As such these RS-plus codes must not be used in hard drives
Remarks on RS-plus Iterative Architecture

- While RS-plus iterative codes perform better with weaker outer RS ECC code (t=12) in random noise environment, extremely poor performance of such ECC under media defects rules out the use of RS-plus iterative architecture in conjunction with weak outer RS ECC.

- With strong outer RS ECC (t=24), the gains under random noise are small, 0.2-0.3 dB. Moreover the performance under media defects is still poor and lagging behind the existing detectors.
• Is it possible to find good RS-plus codes that yield improvement under random noise as well as under media defects?

• The answer is yes. The performance of one such code is shown in the next couple of slides
Viable RS-plus Iterative Architecture

- This RS-plus iterative code gains 0.5dB over state of the art 60/61 SPC code
Viable RS-plus Iterative Architecture

defect length 50 bits, attenuation alpha=0.5
Perp. channel, NPV=[4,7,1], UBD=1.1, jitter=90%, RS-less Iterative Architecture

- The gains of this RS-plus iterative code are largely preserved in media defect dominated noise environment
RS-less Iterative Architecture Class

Iterative Code encoder → Channel

(3,x) LDPC code, where $x \in \{2,3\}$
Code rate = .8974

Min-Sum Iterative Code decoder

3 Inner iterations

SOVA

5 Outer iterations
• RS-less code gains
  ~5.1dB over 60/61
  SPC + RS(t=24) at
  SyER=1e-4
RS-less Iterative Architecture

- RS-less code gains ~1.7dB over 60/61 SPC + RS(t=24) at SER=1e-4

- Need to worry about possible error-floor, to make sure that gains do not vanish at higher SNR’s
RS-less Iterative Architecture

defect length 50 bits, attenuation alpha=0.5
Perp. channel, NPV=[4,7,1], UBD=1.1, jitter=90%, RS-less Iterative Architecture

- RS-less iterative code perform poorly with media defects
Remarks on RS-less Iterative Architecture

• **Pros**
  – Don’t need to worry about compatibility with outer RS ECC
  – Larger SNR gains compared to RS-plus iterative architecture in random noise environment

• **Cons**
  – Poor performance with media defects
  – No reliable analytical techniques to predict system error rate. Some progress have been achieved (e.g. work of Richardson & Urbanke), but the behavior of iterative decoder is still not fully understood.
  – Decoder area tend to be significantly larger and more power hungry compared to RS-plus iterative architecture
Concluding Remarks

• RS-plus iterative code seems to be more attractive for iterative architecture début: strong outer RS code makes the system less sensitive to media defects and other non-standard noise sources.

• Well designed RS-plus architecture outperforms state of the art non-iterative detector in random noise as well as media defect dominated environment.

• More research is necessary for RS-less architecture before it can be incorporated into the product.