Cutting Power Consumption in HDD Electronics

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Situation Overview

- The industry continues to drive to lower power solutions
  - Driven by:
    - Need for higher reliability
    - Extended battery life for mobile and handheld devices
  - Performance requirements continue to increase
- Being competitive requires IP directed at reducing power consumption
  - Process shrink is an enabler, but not the driver
  - Innovations focused in two key pieces of IP
    - Read channels
    - Serial interface
Storage IC Technology Explained

System on a Chip (SoC)

- Host
- Interface Controller
- Read Channel
- Memory
- Hard Disk Controller
- Motor Controller
- External Memory
- Preamp
- Spindle Motor
- Disk Platter
- VCM
- Read/Write Head
Sample HDD Power Budget

- Roughly $\frac{1}{2}$ the budget is electronics
  - A large opportunity for improving power savings
Reliability Driver

- With higher data rates, increasing the power in a given form factor increases temperature
  - Decreases inherent electronics reliability
    - Failure rate is exponential with temp
  - Results in a rich system failure pareto
    - head / disk failures in the system
    - ...

- Decreasing power (temperature) improves reliability
Extending Battery Life

- Major factor in handheld devices
  - Translates into extended ‘live-time’
- In order to minimize storage power the host utilizes a data buffer:
  - Reduces on-time of HDD
- With advent of video:
  - Battery ‘live-time’ expectation set from audio
    - Reduce power dramatically and/or
    - Increase buffer size – costs more
- Must reduce storage power and operate at low battery voltage

[Diagram showing operation time and battery voltage characteristics with examples of HDD, DRAM Buffer, and MP3 or MPEG.]
Process-Enabled Power Reduction

- Reduction in operating power through process shrink:
  - Dynamic power shrinks with process
    - Applies to digital logic
    - Analog doesn’t scale
  - Resulting mixed signal power reduction is less.

- Additional wrinkle:
  - Leakage current increases with process shrink
  - With finer geometries, leakage becomes more significant.

\[
\text{Dynamic Power} = C V^2 f
\]
Handheld Device Challenge

- Leakage power is an important aspect of battery-operated handheld devices
  - Standby mode needs extremely low power
- Requires higher threshold devices
  - Thresholds required for 65 nm are high, requiring a high core voltage
- Cannot take full advantage of:
  - $\text{(Core Voltage)}^2$ related power reduction
- Drives the need for innovation in:
  - Process
  - Architecture
  - Implementation
HDD Performance Impacting Power Consumption

- HDD transfer rates driven by density increases:
  - Every double of capacity results in:
    ~1.4X transfer rate
    ~1.4X number of servo fields
  - Results in channel clocks scaling proportionally and processor speed requirements increasing.

- Driving towards increased ECC capabilities
  - Results in more area/logic.

- All of these increase power...
• New 90 nanometer read channel designs offer 70 percent power reduction over 130 nm

• The IP improvements are architectural in scope across all product segments

• Power optimization must preserve signal-to-noise ratio performance
Serial Interface Adoption Impacting Power Consumption

- Seeing adoption of High-speed SATA interface across product segments:
  - Used widely in desktop drives
    - Desktop is converging on 3 Gb/s
  - Transitioning to the mobile market
    - ~1 year behind desktop
    - Mobile will probably hold at 1.5 Gb/s for the near term due to power sensitivity
  - Enterprise will spearhead 6 Gb/s on SAS (~2008)

- Most significant power consuming block is the Physical Layer Interface block (PHY)

- Data rates are moving higher, so how can we maintain or reduce power budgets?
Power Solutions - Serial Interface PHY

- New 90 nm serial PHY’s offering 40 percent power reduction over 130 nm design
- Still able to produce performance improvements (6 Gb/s)
Summary – Mixed Signal Power

- Increasing Performance requirements, Reliability and Battery live-time push the need for power reduction.
- Mixed signal analog power improvements are best addressed by design innovation.
  - Target architectural improvements to span product segments
- HDD silicon and system manufacturers will continue to be challenged to reduce or maintain power.
  - Be aligned with a silicon provider producing the necessary innovation.
IDEMA
Advances in HDD Electronics
December, 2005
Dave Mosley
VP – Emerging Products Development
A multitude of technologies have been used to enable dramatic reductions in the footprint and power of HDD electronics!
HDD Electronics Advances

- Silicon Integration
- ECC
- Packaging
- Buffer memory utilization
- Functional Integration

- Combine controller, formatter & glue logic
- Embed SRAM

- Pull read channel into SoC
- Incorporate voltage regulators into spindle control device
- Eliminate flash by storing code on disc

- Embed DRAM in SoC
- Reduce Power to allow SoC
- Reduce Pads/connections
HDD Electronics Advances

- **Silicon Integration**
- **ECC**
- **Packaging**
- **Buffer memory utilization**
- **Functional Integration**

Gains made with improved ECC schemes enable the use of *smaller* less powerful read channels.

- Faster DRAM
- Code moved from Flash to Disc. Executed out of DRAM
- Faster DRAM enabled smaller SRAM which was moved internal to SoC
- Future designs will have the DRAM buffer embedded in the SoC. This supports very high bandwidth and very low power.

**Gains made with improved ECC schemes**

Du=2.0, 18-22dB, 90% Jitter, S=10, I=1

- 69/70 CCE vs 30/31 ECC,
  - Du=2.0, 18dB
  - Du=2.0, 19dB
  - Du=2.0, 20dB
  - Du=2.0, 21dB

- 30/31 ECC
  - Du=2.0, 19dB
  - Du=2.0, 20dB
  - Du=2.0, 21dB

**Correction capability, T**

- CBER (Sector per bit)
- Gain in error rates with reverse ECC
HDD Electronics Advances

- Silicon Integration
- ECC
- Packaging
- Buffer memory utilization
- Functional Integration

TQFP

COB

Flip Chip
Optimization at the system level is the key to the future!

HDD optimization is reaching its minimum point

The answer is.....

AND

The storage device is the largest factor to BOM cost in many CE devices

Optimize the system around the storage device!

• Functional integration of system and storage device(s)
• Fully utilize HDD electronics to eliminate redundant system functions
• Take an HDD centric approach to optimize system BOM cost and reduce power usage
• Allows more flexibility for data
  – Storage
  – Usage and delivery

PMP BOM Cost Break-down

- HDD 54%
- LCD 19%
- Application Electronics 20%
- Battery 2%
- Mechanical 5%

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What's next: Increased functionality in the HDD!

In a typical compressed audio player the HDD is spun up and transferring data less than 1% of the time.

- In many systems the processing capability of the HDD electronics is predominantly idle.
- Future system design will take advantage of this available capability; moving more functionality into the HDD and further minimizing the overall design.

An average personal video player has the HDD active only 5 seconds out of every 11 minutes.
Optimized Semiconductor
Process Choices for Mixed-Signal
HDD Devices

Deames Davis
Manager, Marketing/
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Myths about Mixed-signal Processes

• Device in next generation process is always:
  - Smaller die size
  - Lower cost
  - Better power handling
  - Better performance
# HDD Segment Considerations

<table>
<thead>
<tr>
<th>Segment</th>
<th>Cost</th>
<th>Die Size</th>
<th>Power</th>
<th>Performance</th>
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<tr>
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<td>Microdrive</td>
<td>3</td>
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Die Size Impact

• Minimum feature size shrinks with each successive process node
• Digital functions get full entitlement of shrink
• Analog functions are sized based on voltage/current requirements
  – Many analog functions need transistors larger than minimum-feature-size
  – Die area for given block may not change in successive process nodes
• Die size reduction is probable, but not guaranteed
Mixed-Signal Process Roadmap Enables Increased Integration, Performance, and Functionality

Ex: 12V Combo Motor Driver IC

- Mixed-signal lithography follows in digital process footsteps
- Smaller chip plus increased integration
  - Preamp: Head Heaters, ADCs, Vertical Recording, etc.
  - Servo: Dual Stage Actuation, Shock interface, Vreg FETs, etc.

12/06/05
Deames Davis
Cost Impact

• Wafer prices tend to be set by complexity
  – Mask levels, process steps, etc.
  – Metallization technology
  – Manufacturing cycle time is also set by complexity

• New processes may need new fab equipment
  – Depreciation cost
  – Highest cost during early production

• Volume/time will reduce cost, but device cost at process transition is ~parity
Power Impact

• **Dissipation**
  - For like feature set and performance, device in next generation process tends to use less power

• **Power Density**
  - Processes can be optimized to handle higher power density (e.g. top-layer copper)

• **Handling**
  - Small die handles less power than larger die due to less physical contact with thermal path
Conclusions

• Device in next generation process is **always**:
  - Smaller die size (Mostly, Yes)
  - Lower cost (Over time, Yes)
  - Better power handling (Match power to die size)
  - Better performance (Mostly, Yes)

• Process choice involves trade-offs and timing within process life-cycle

• It is important to have a “quiver” of processes to provide the right process for the right product
  - Need to consider all aspects of performance (speed, power, voltage, current) before choosing process